SN74LS175N

Product Introduction

The SN74LS175N is a Hex/Quad D Flip-Flops with Clear.It is positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input,Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The 4 groups share a reset input and a clock input.

Product Features

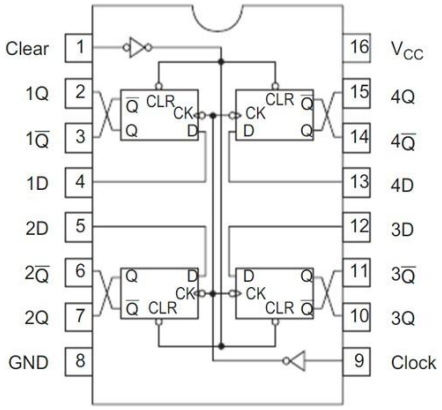
- Hex/Quad D Flip-Flops with Clear.
- Fully compatible with TTL/DTL input logic level
- Share a reset input and a clock input
- Have Complementary output function
- Package format: DIP16, SOP16

Product Applications

- Digital logic driver
- Industrial control application
- Other application areas

Package and Pin Assignment

SOP16 or DIP16			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Clear	16	Supply VCC
2	Output 1Q	15	Output 4Q
3	Output 1$\overline{Q}$	14	Output 4$\overline{Q}$
4	Input 1D	13	Input 4D
5	Input 2D	12	Input 3D
6	Output 2$\overline{Q}$	11	Output 3$\overline{Q}$
7	Output 2Q	10	Output 3Q
8	Supply GND	9	Clock

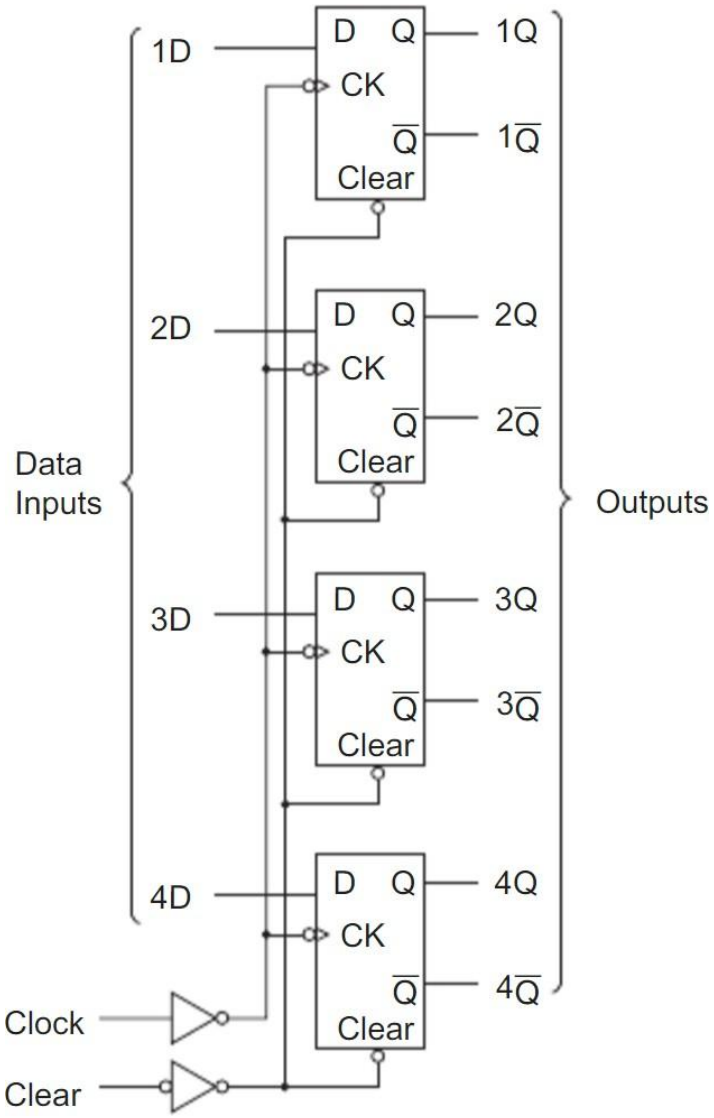


Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Welding temperature	T_W	260,10s	℃

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

■ Block Diagram



■ Function Table

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H= High Level (steady state) ; L=Low Level (steady state); X = Don't Care;

↑ =Transition from low to high level

Q0= The level of Q before the indicated steady-state input conditions were established.

Recommended Operating Conditions

Item		Symbol	Min	Tpy	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	uA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	0	—	60	℃
Clock frequency		fclock	0	—	30	MHz
Clock pulse width		$T_{W\ (CLK)}$	20	—	—	ns
Clear pulse width		$T_{W(CLR)}$	20	—	—	ns
Hold time		th	5	—	—	ns
Setup time	D input	tsu	20	—	—	ns
	Clear(in active state)		25	—	—	ns

Electrical Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage	V_{IH}	2	—	—	V		
	V_{IL}	—	—	0.8	V		
Output voltage	V_{OH}	2.7	3.3	—	V	I_{OH}=-400uA	VCC=4.75V,V_{IH}=2V , V_{IL}=0.8V
	V_{OL}	—	0.12	0.4	V	I_{OL}=4mA	
		—	0.20	0.5		I_{OL}=8mA	
Input current	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	I_{IL}	—	0.25	-0.4	mA	VCC=5.25V, V_I=0.4V	
	I_I	—	0.1	100	uA	VCC=5.25V, V_I=7V	
Short-circuit output current *	I_{OS}	-20	-35	-100	mA	VCC=5.25V	
Supply current**	I_{CC}	—	9	18	mA	VCC=5.25V	
Input clamp voltage	V_{IK}	—	0.9	-1.5	V	VCC=4.75V, I_I =–18mA	

Notes:* only one output port is short circuited each time, and the short circuit time is not more than one second.

**With all outputs open and 4.5 V applied to all data and cleat inputs, ICC is measured after a momentary grounded, then 4.5V, is applied to clock.

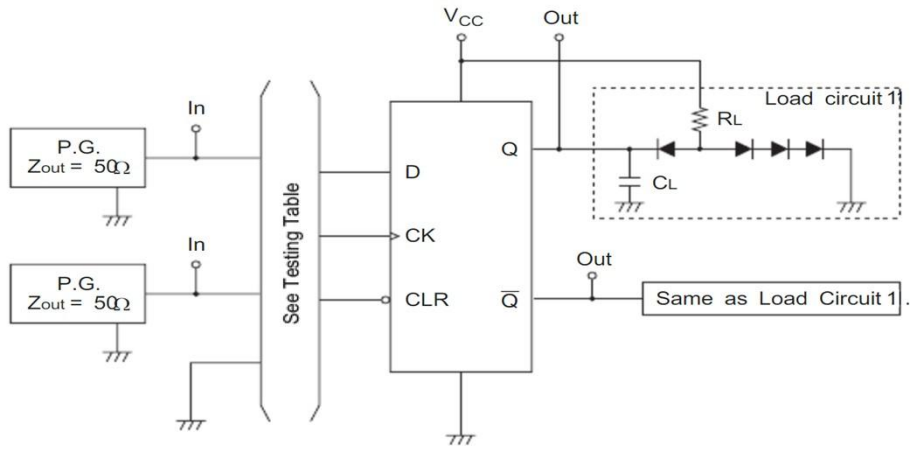
Switching Characteristics

(T_A=25℃, Unless specified)

Item	Symbol	Min	Tpy	Max	Unit	Conditions
Maximum clock frequency	fmax	0	25	—	MHz	V_{CC}=5V,C_L=16pF, R_L=2K
Propagation delay time Clock to Q	t_{PLH}	—	14	—	ns	
	t_{PHL}	—	20	—	ns	
Propagation delay time Clear to $\overline{Q}$	t_{PLH}	—	16	—	ns	
Propagation delay time Clear to Q	t_{PHL}	—	27	—	ns	

■ Testing Method

1、Test Circuit



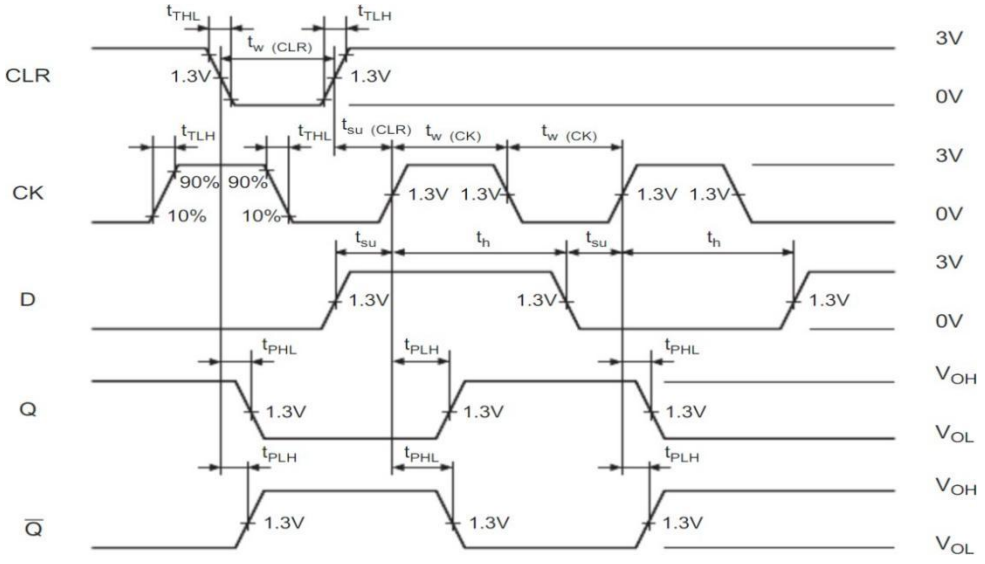
Notes:

1. See Testing Table refers to the corresponding test items in the switch characteristic table.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND. All diode models are 1S2074 (H).
3. Input: port input level, f=1MHz, D=50%, tTHL=tTLH =20ns;

2、Testing Table

Item	From input to output	Inputs			Outputs	
		CLR	CK	D	Q	$\overline{Q}$
f_{max}	CK→Q, $\overline{Q}$	4.5 V	IN	IN	OUT	OUT
t_{PLH}	CK→Q, $\overline{Q}$	4.5 V	IN	IN		
t_{PHL}	CLR→Q, $\overline{Q}$	IN	IN	4.5 V		

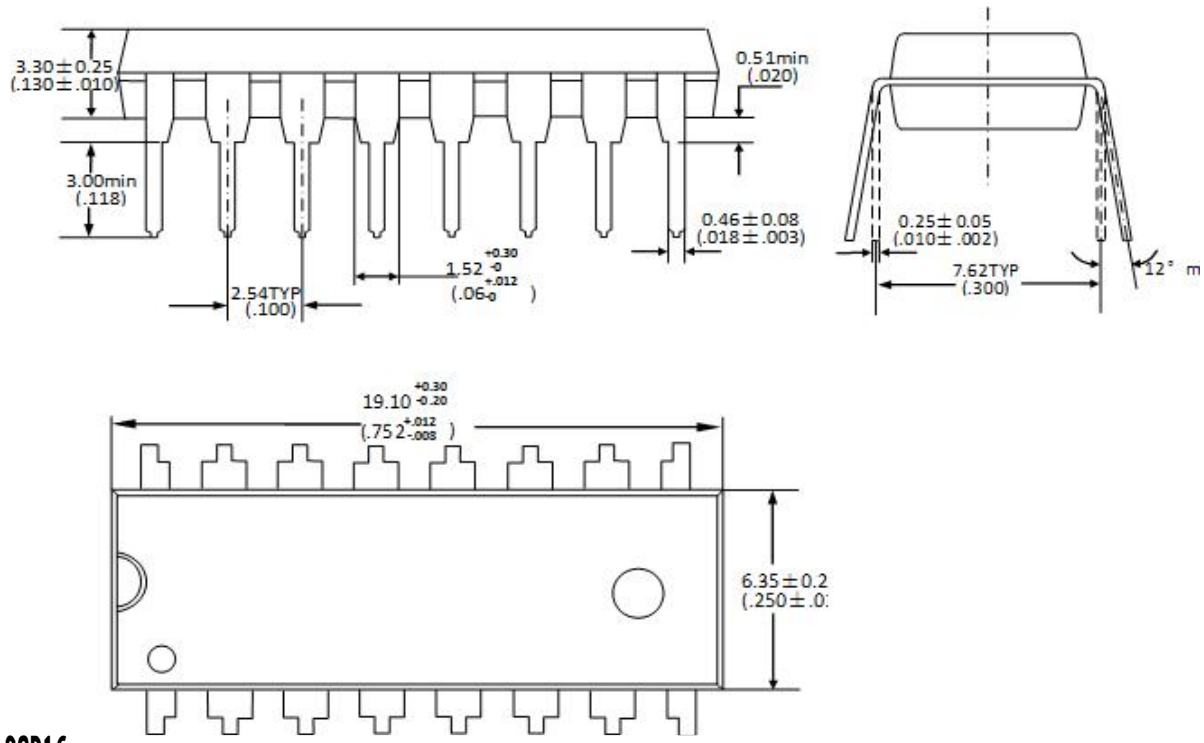
3、Waveform



■ Package Dimensions

Unit：mm /inch

DIP16



SOP16